

Fig.1

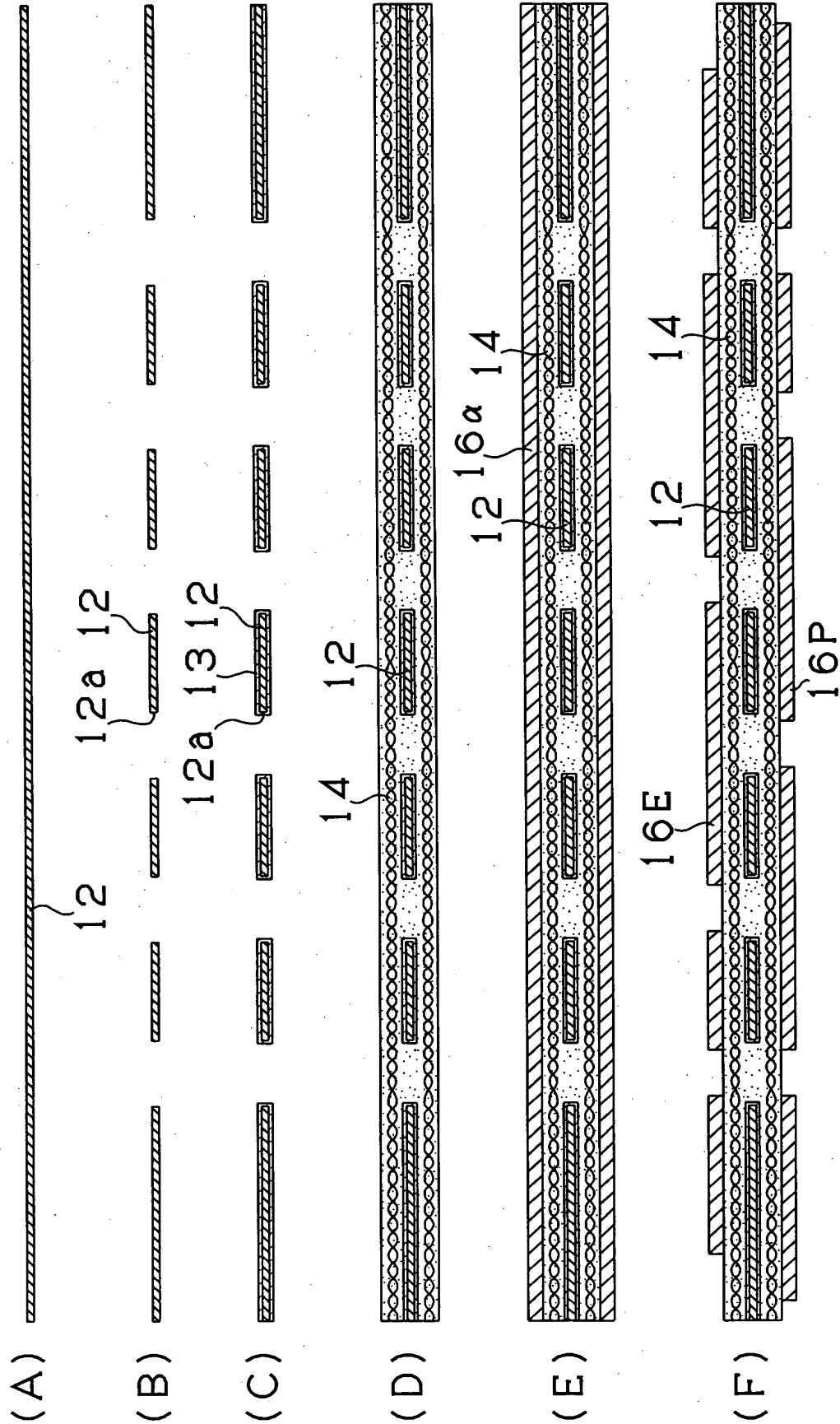
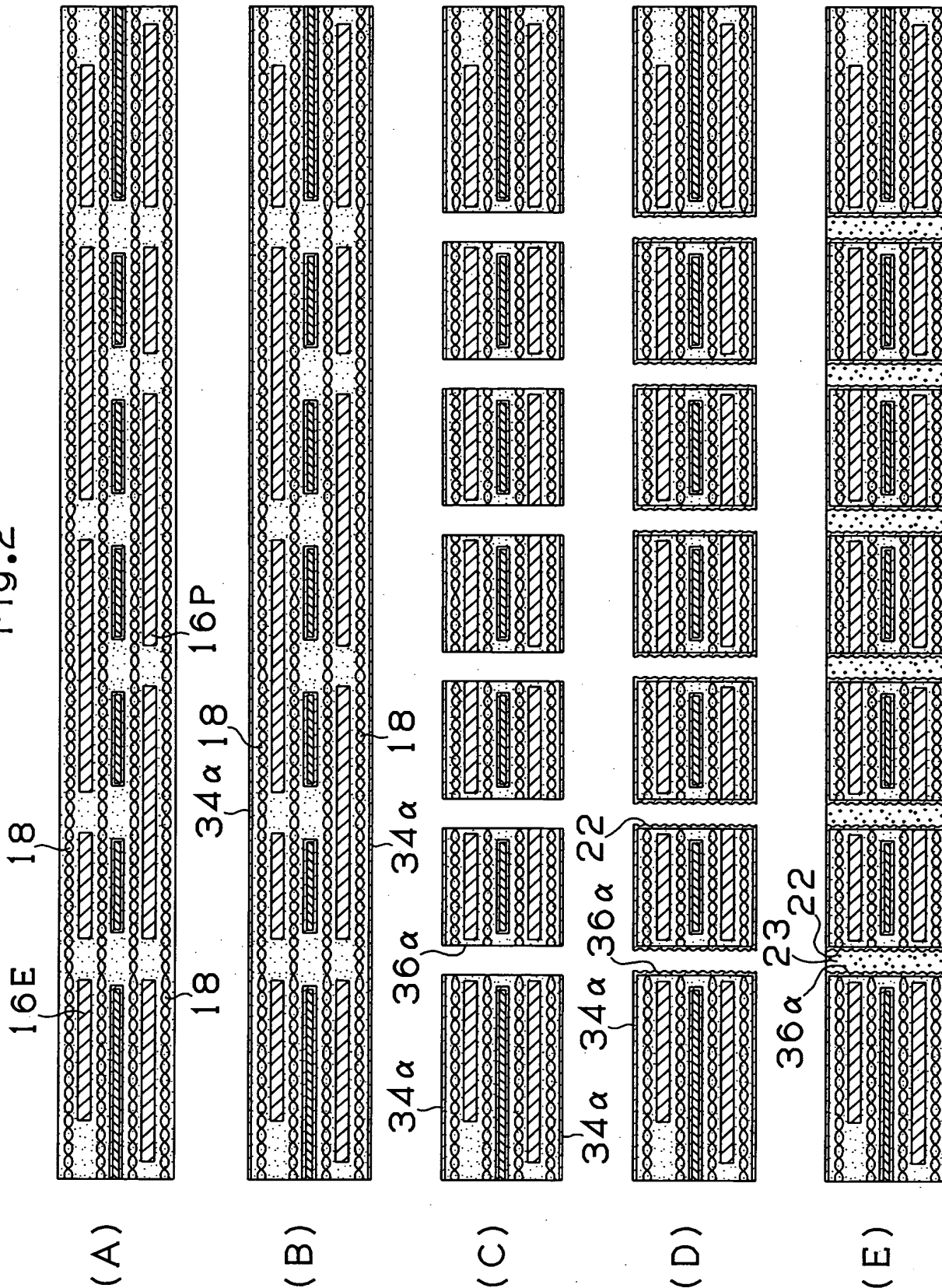


Fig.2

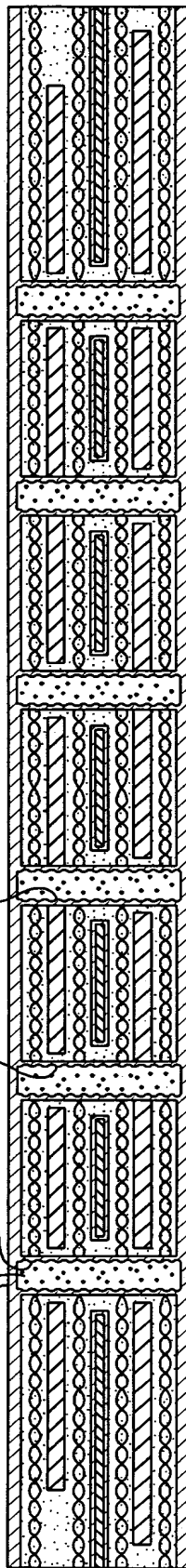


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Fig. 3

(A)

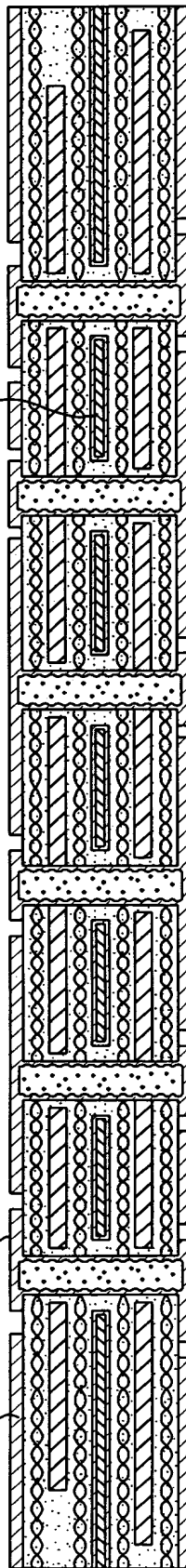
25 23 36S 36P 36E



(B)

34P 34

30



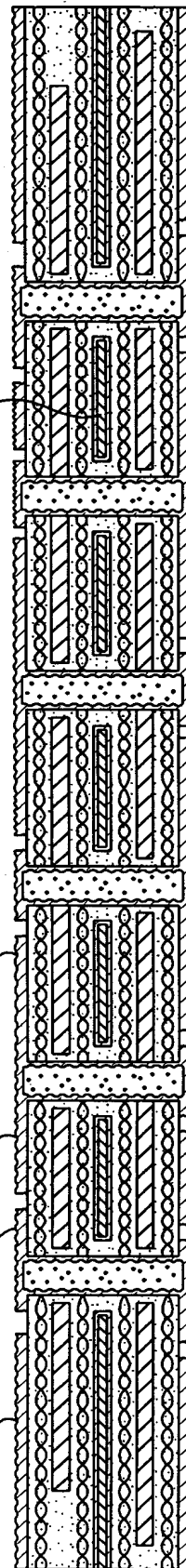
(C)

34P 34 34B

30

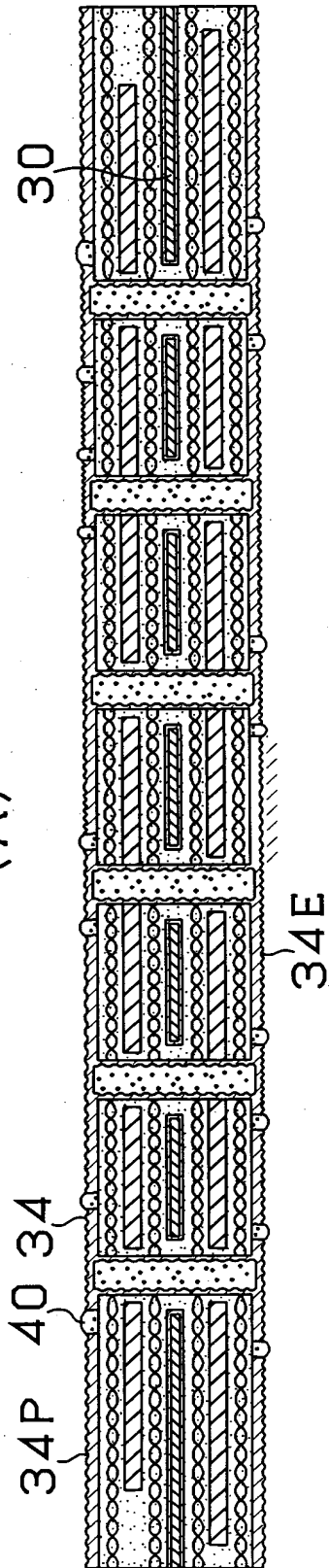
34E

34E

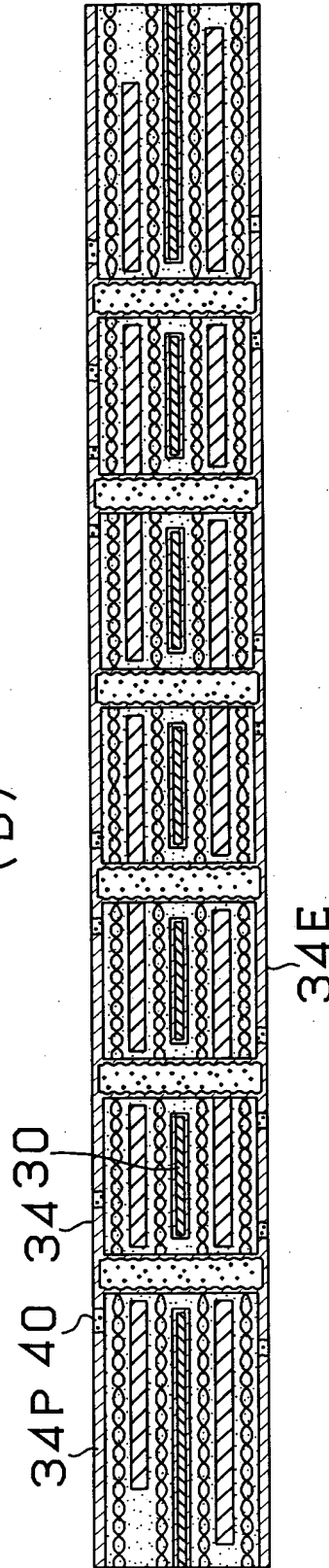


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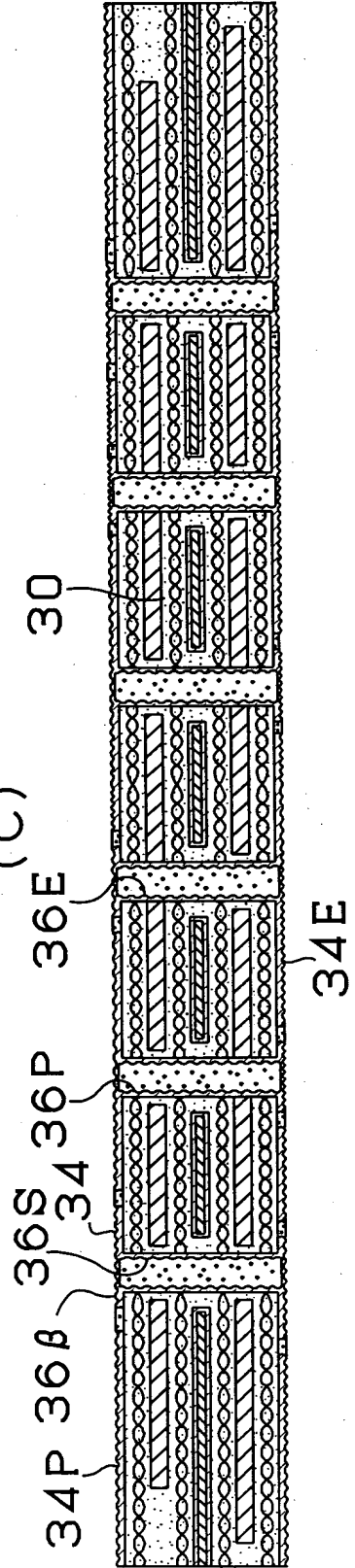
Fig. 4
(A)



(B)



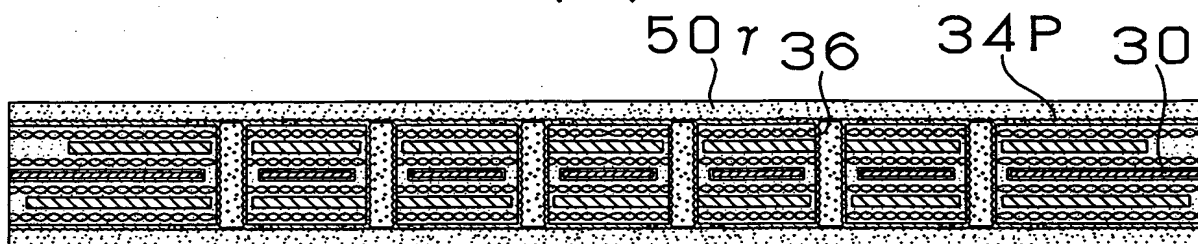
(C)



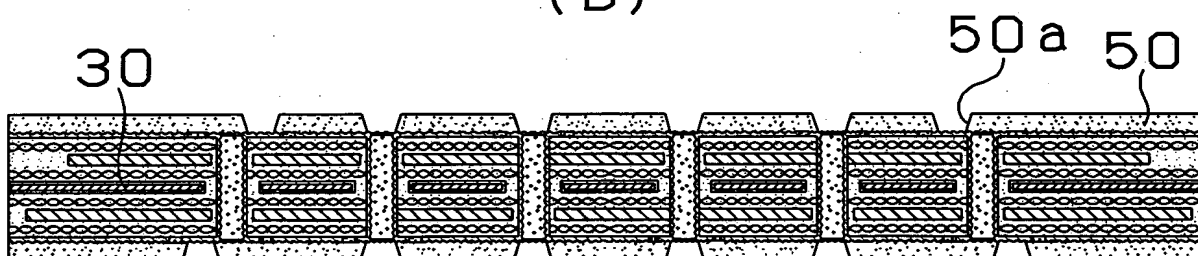
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Fig. 5

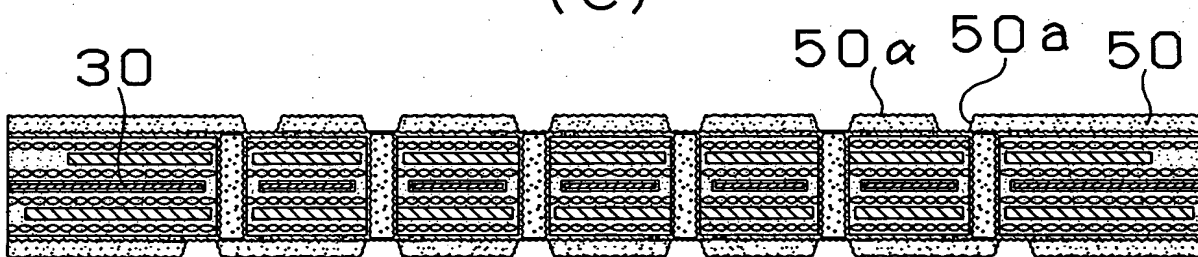
(A)



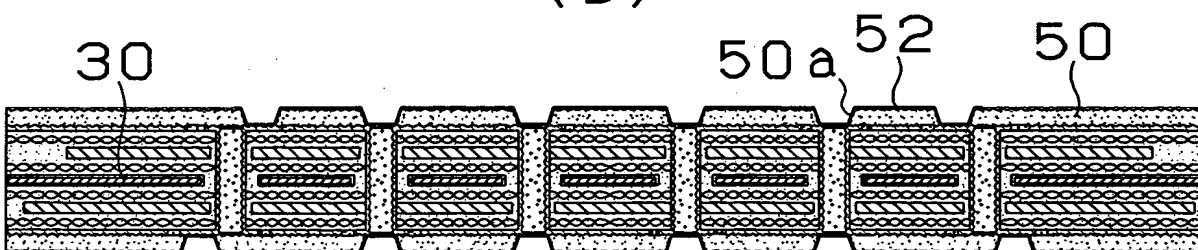
(B)



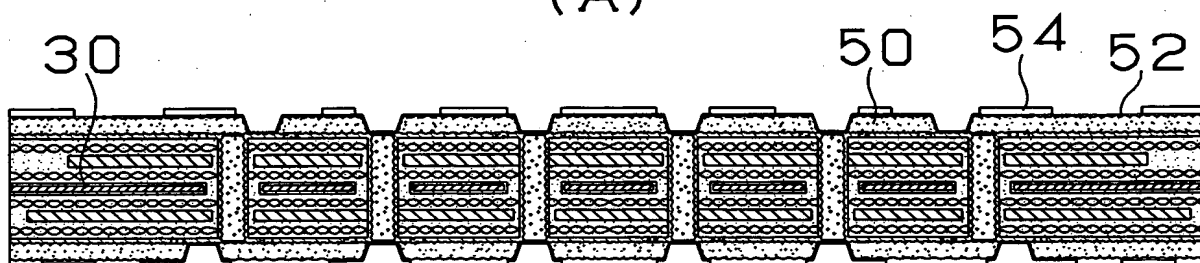
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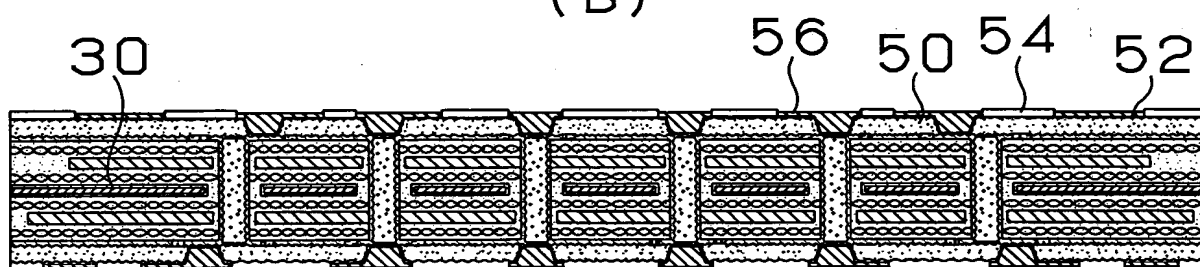
(D)



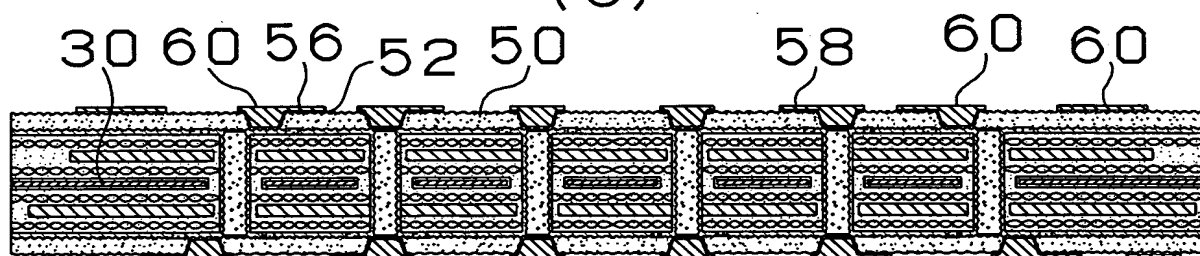
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Fig.6
(A)



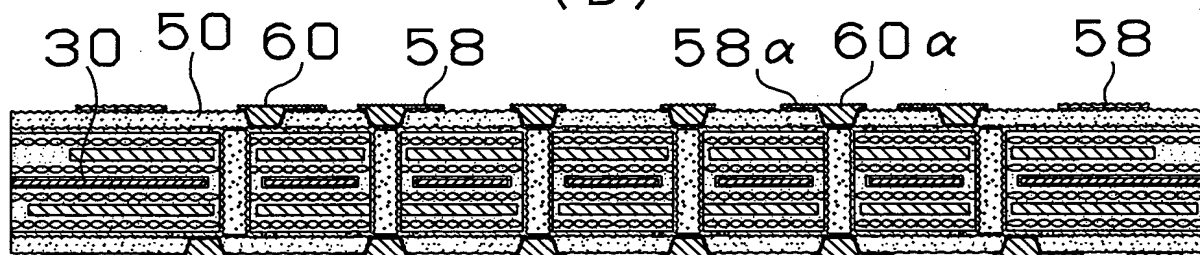
(B)



(C)



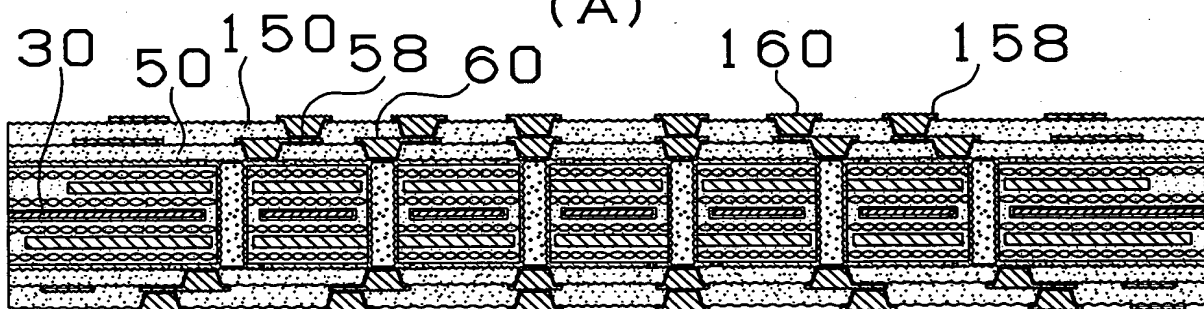
(D)



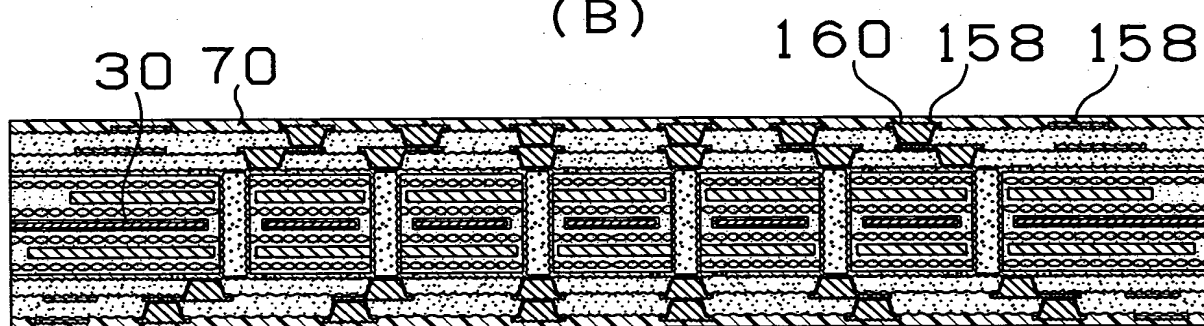
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Fig. 7

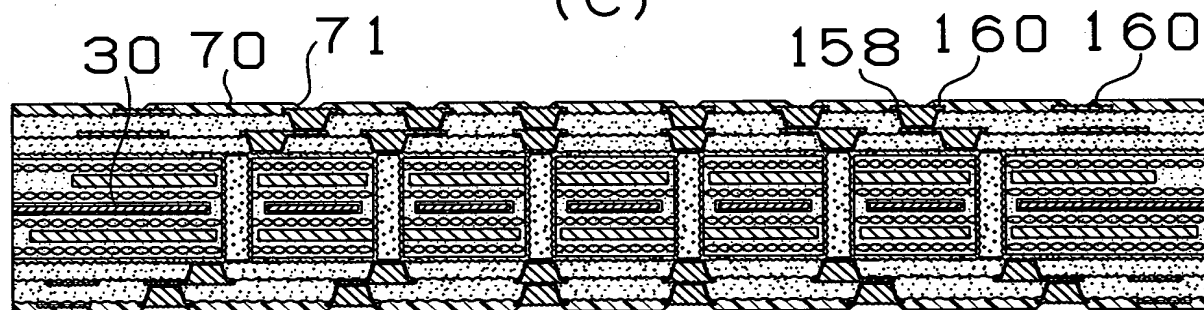
(A)



(B)



(C)



(D)

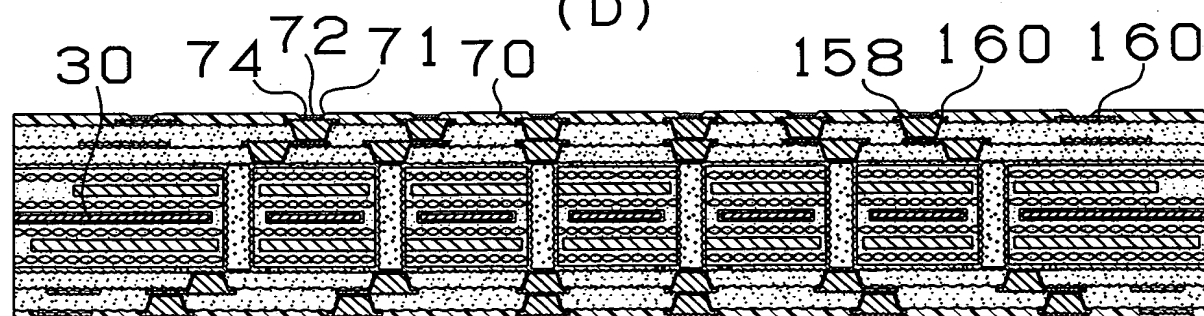
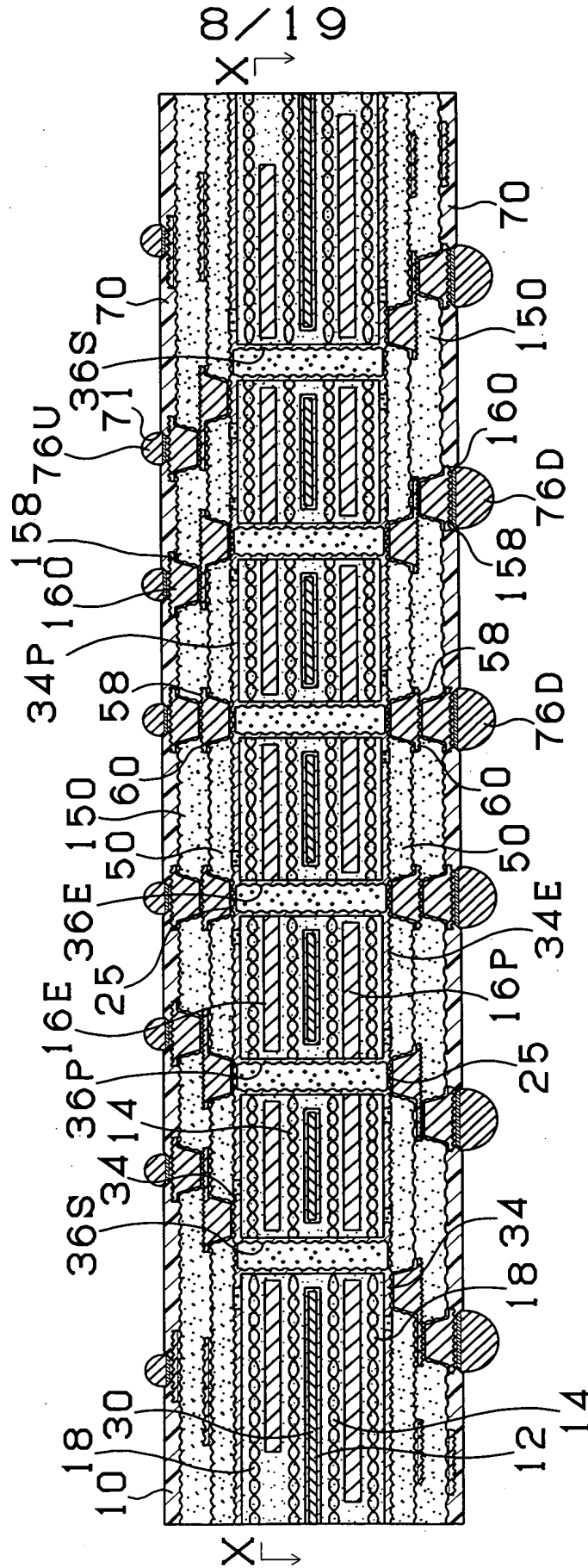
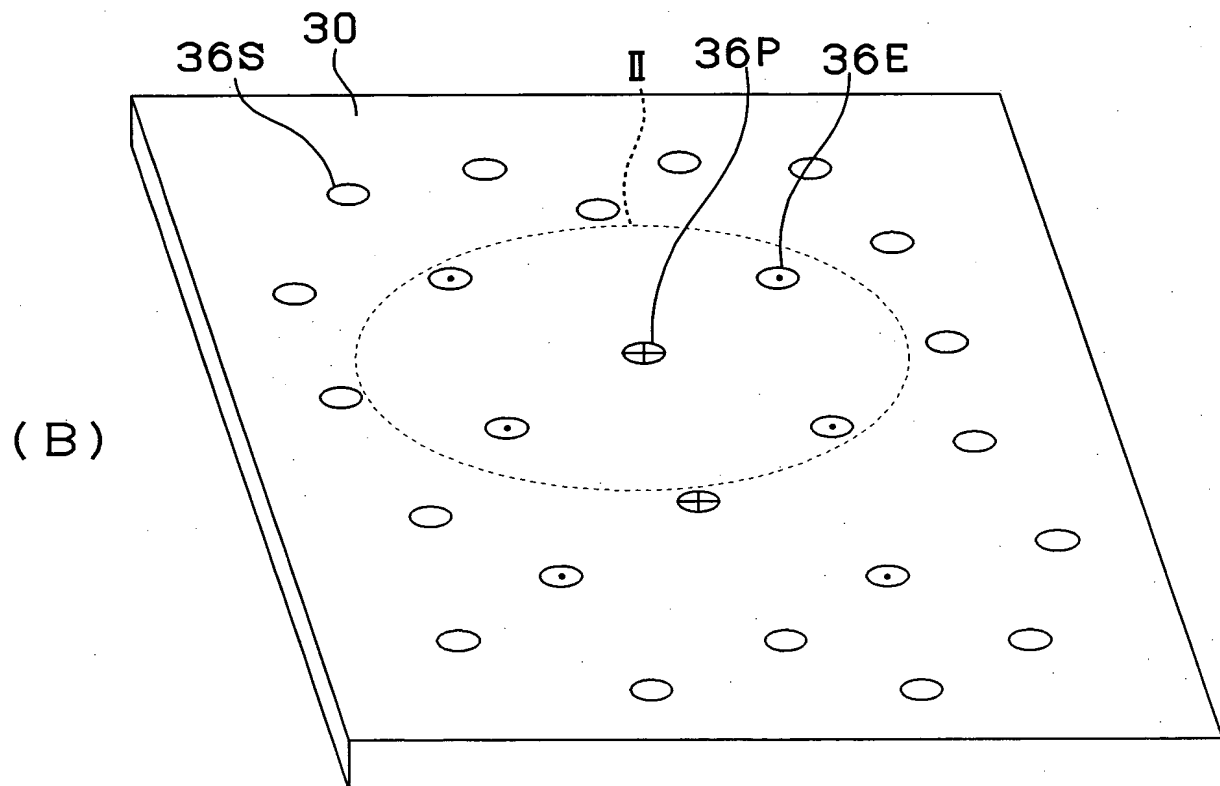
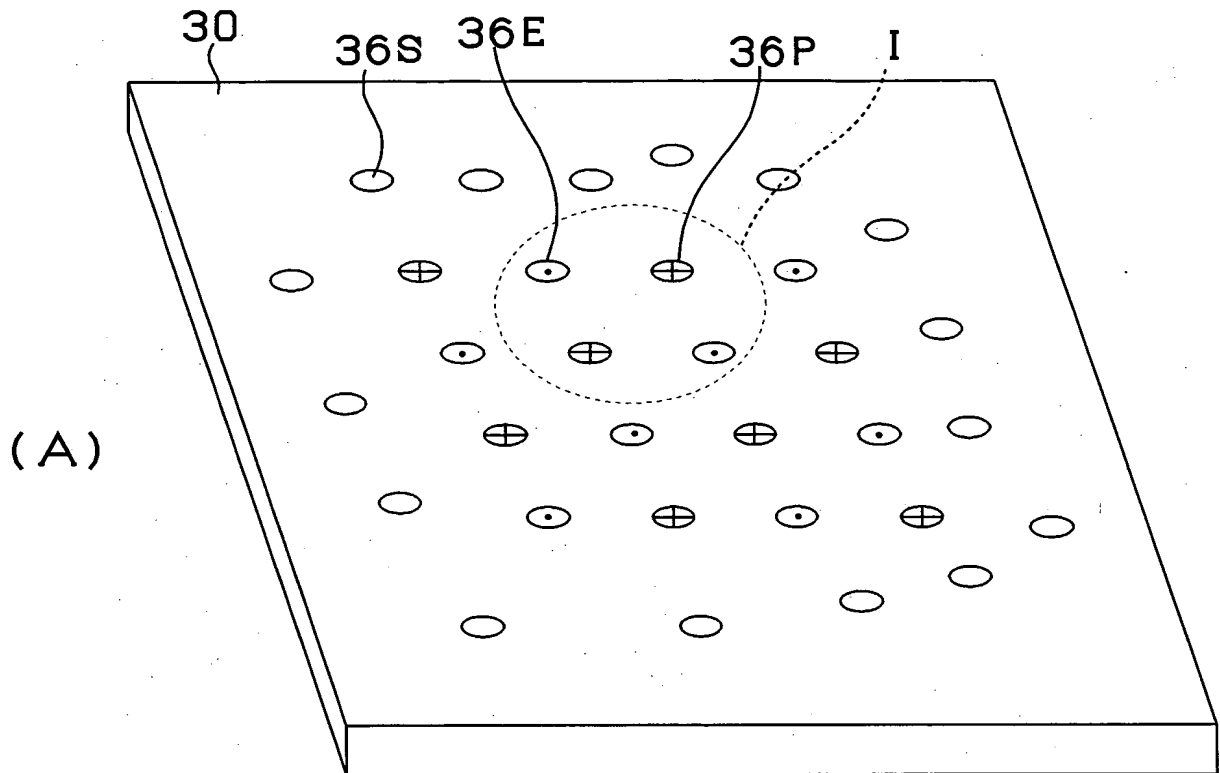


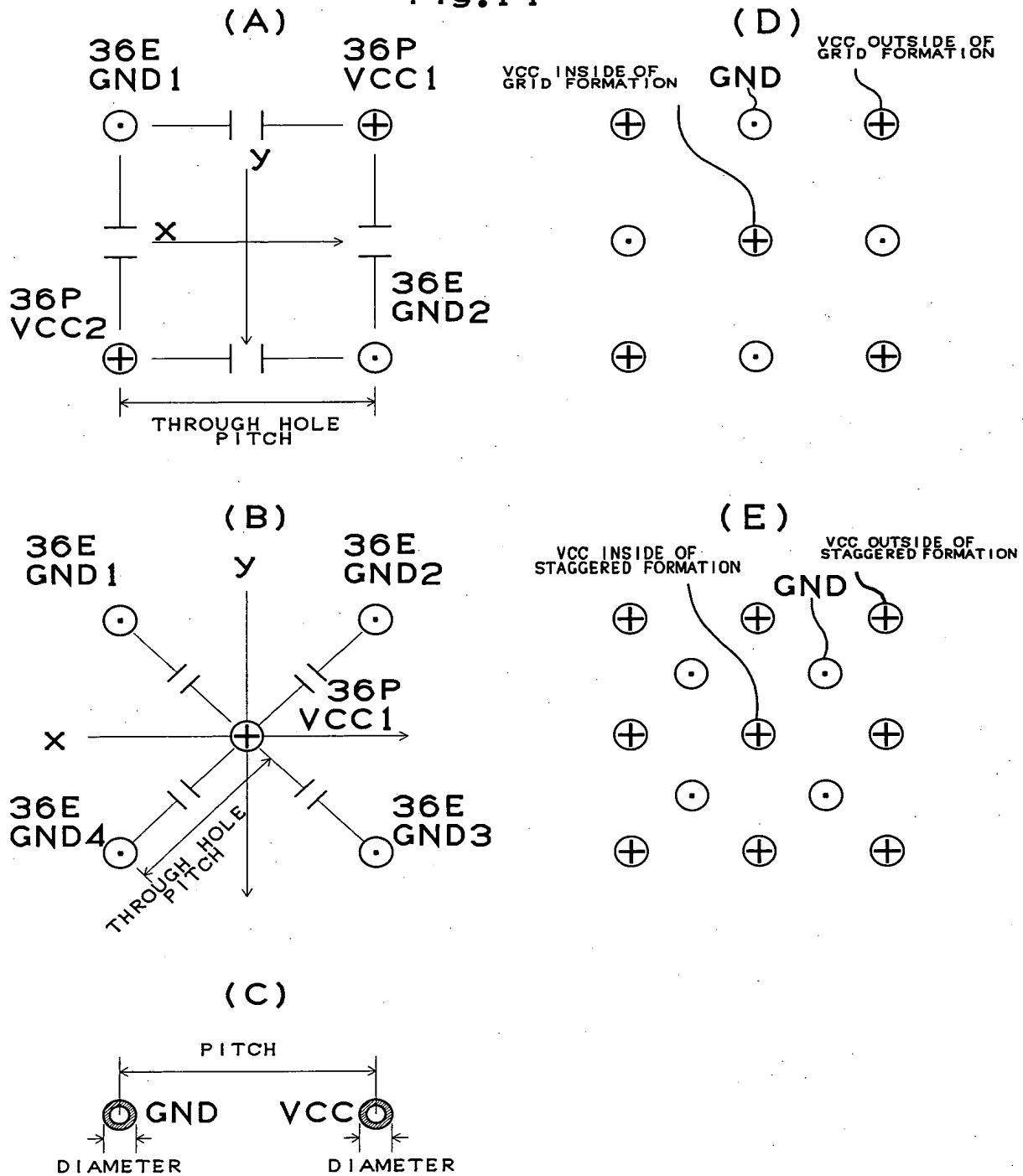
Fig. 8



This cross-sectional view shows a multi-layered semiconductor device. At the top, there is a layer labeled 36S. Below it is a layer labeled 36P. A central region is labeled 90. Within this central region, there are several layers: 92S, 92E, and 92P. Below these is another layer labeled 36P. The bottom-most layer is labeled 36S. On the right side, there are labels 96S, 96E, 96P, 76U, 76D, and 94. The diagram uses various hatching patterns to represent different materials or layers.

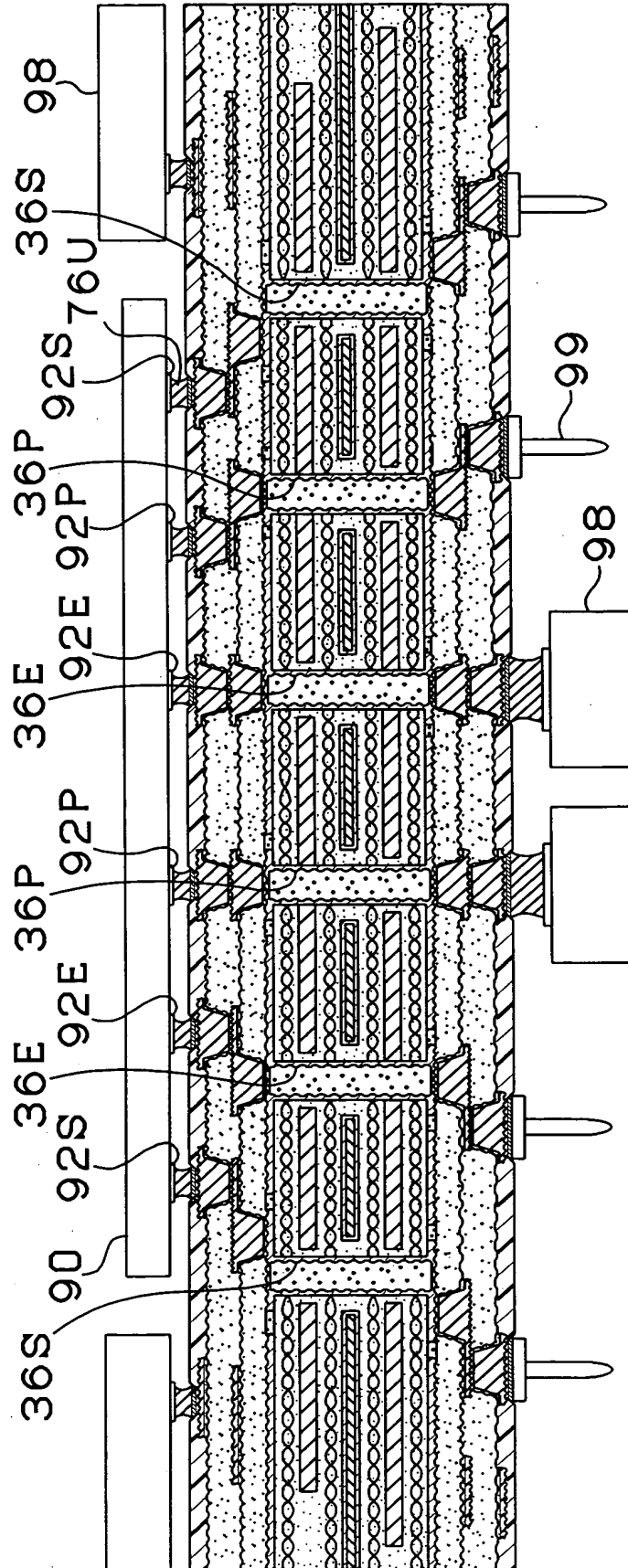
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Fig.10



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Fig. 11

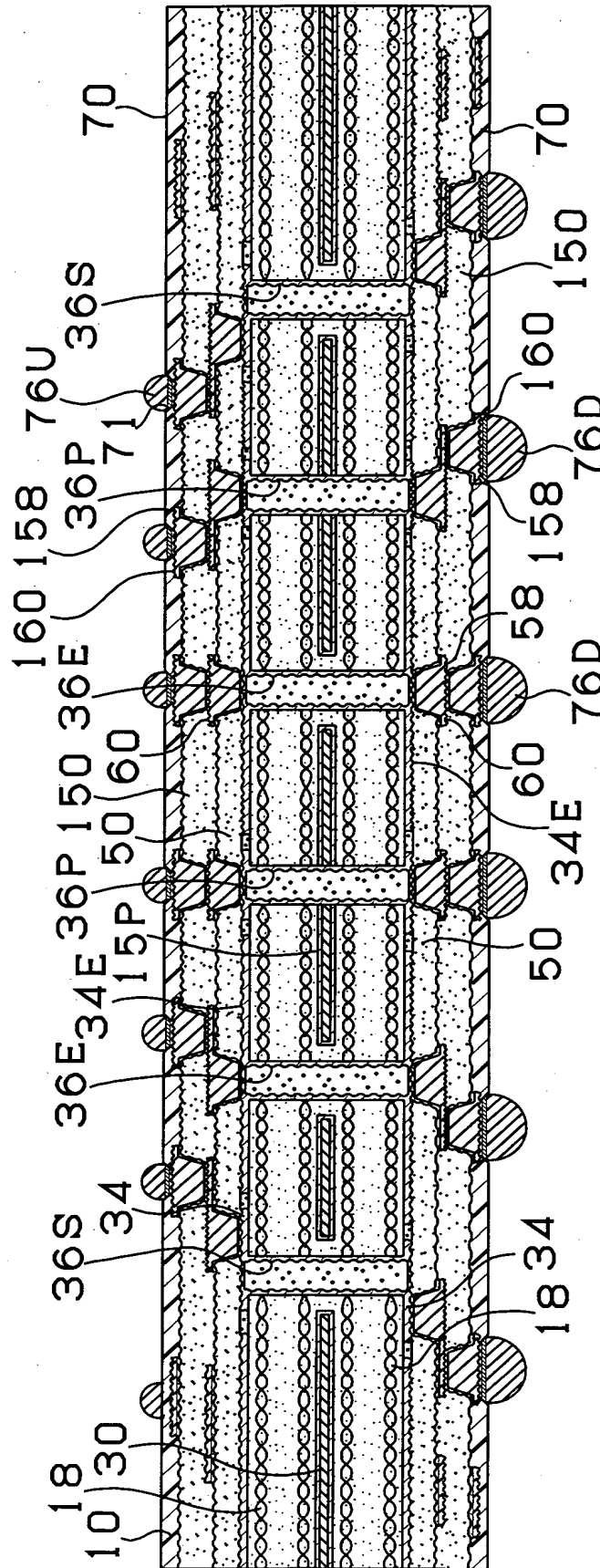
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Fig.12



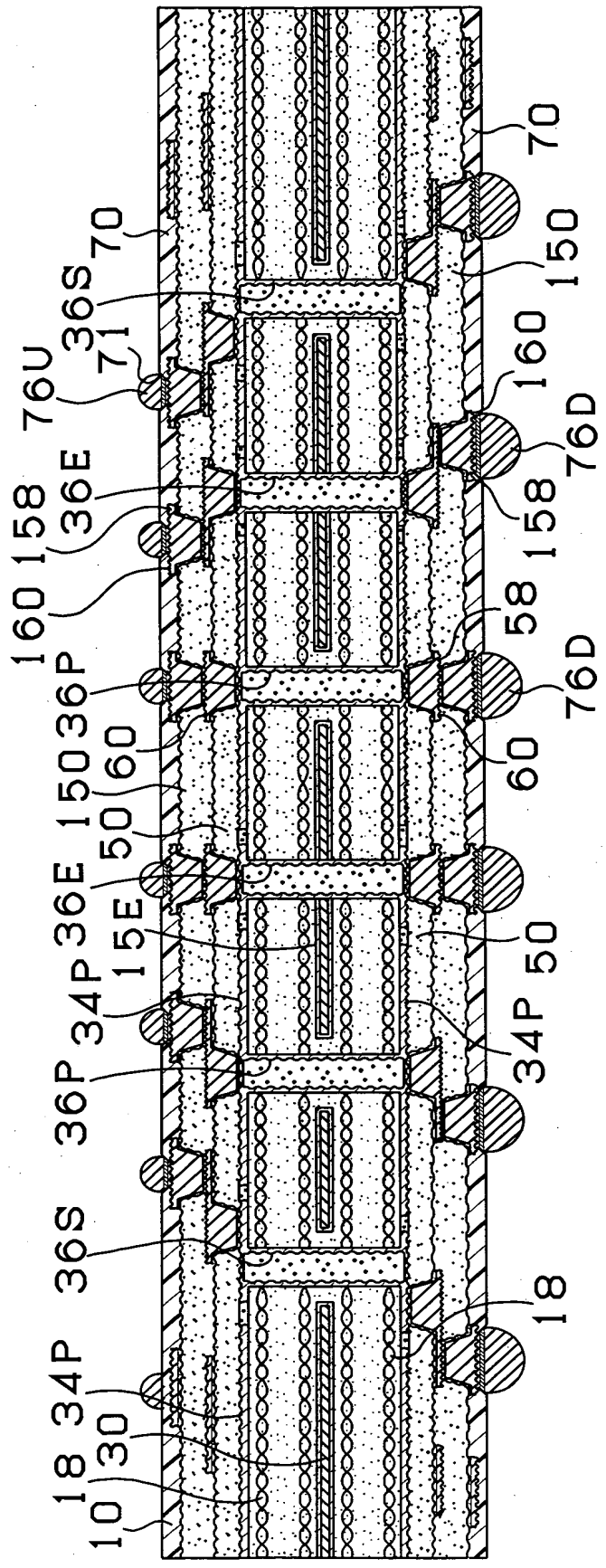
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Fig. 13



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Fig. 14



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Fig.15

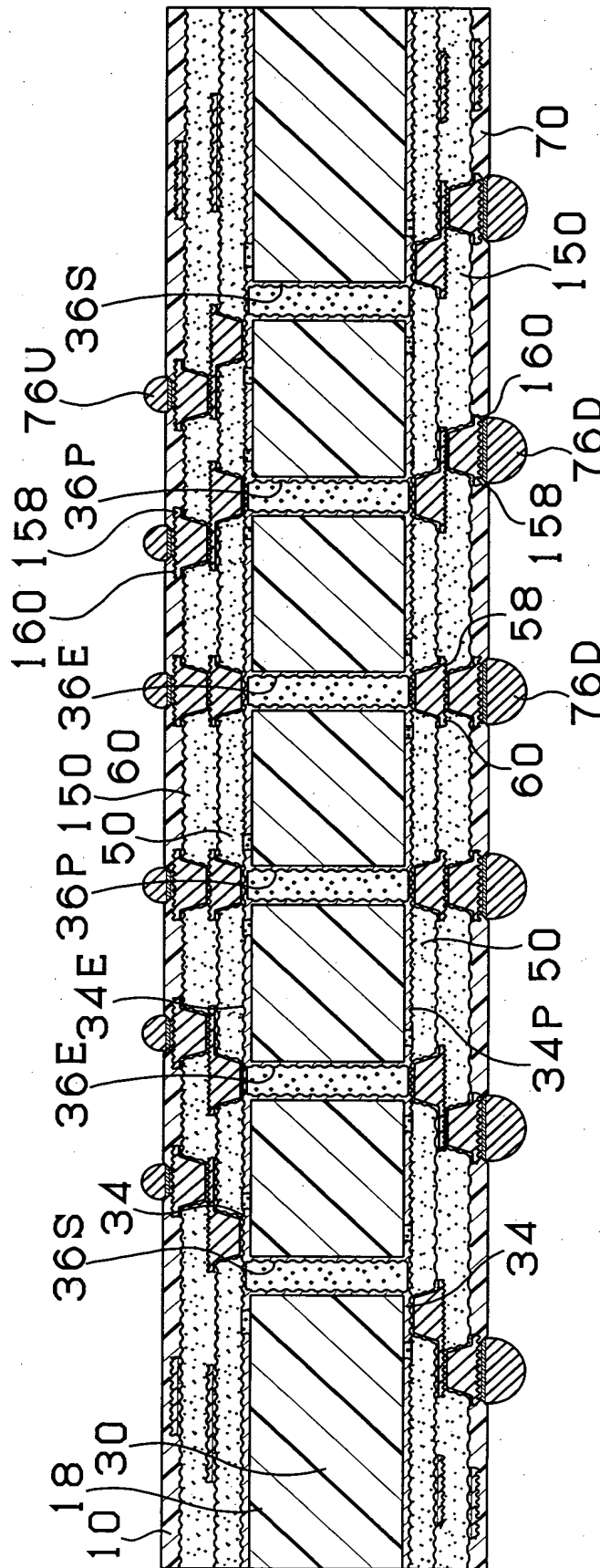


Fig. 16

THROUGH HOLE PITCH (μm)	THROUGH HOLE DIAMETER (μm)	THICKNESS OF CORE SUBSTRATE (μm)	STAGGERED FORMATION (THICK COPPER)	GRID FORMATION	RANDOM FORMATION	FOURTH REFERENCE EXAMPLE
			LOOP INDUCTANCE (pH)	LOOP INDUCTANCE (pH)	LOOP INDUCTANCE (pH)	LOOP INDUCTANCE (pH)
650	450	600	93	84	115	
600	400	600	87	75	109	88
550	350	600	73	59	100	75
500	300	600	73	56	95	75
475	275	600	63	57	90	65
450	250	600	59	55	85	62
425	225	600	58	55	85	60
400	200	600	59	55	—	60
80	50	600	55	50	90	57
50	25	600	63	60	—	

NOTE: A DIFFERENCE BETWEEN FOURTH REFERENCE EXAMPLE AND GRID FORMATION (THICK COPPER) IS JUST A SUM OF THICKNESSES OF CONDUCTIVE LAYERS IN MULTI-LAYER CORE SUBSTRATE.

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Fig. 17
(A)

THROUGH HOEL PITCH (μm)	STAGGERED FORMATION (THICK COPPER)		GRID FORMATION (THICK COPPER)	
	CRACK IN INSULATING LAYER	RESULT OF CONDUCTIVITY TEST	CRACK IN INSULATING LAYER	RESULT OF CONDUCTIVITY TEST
650	○	○	○	○
600	○	○	○	○
500	○	○	○	○
400	○	○	○	○
80	○	○	○	○
50	×	×	×	×

CRACK IN INSULATING LAYER : ○ NO CRACK × CRACK

RESULT OF CONDUCTIVITY TEST : ○ NO ABNORMALITY IN RESISTANCE
× ABNORMALITY IN RESISTANCE

(B)

THROUGH HOEL PITCH (μm)	STAGGERED FORMATION	GRID FORMATION
	LOOP INDUCTANCE (pH)	LOOP INDUCTANCE (pH)
650	93	84
600	87	75
550	73	60
500	63	56
475	63	57
450	59	55
425	58	54
400	55	52
350	54	50
300	54	50
200	53	50
100	54	49
75	54	49
60	55	50
50	63	60

Fig. 18

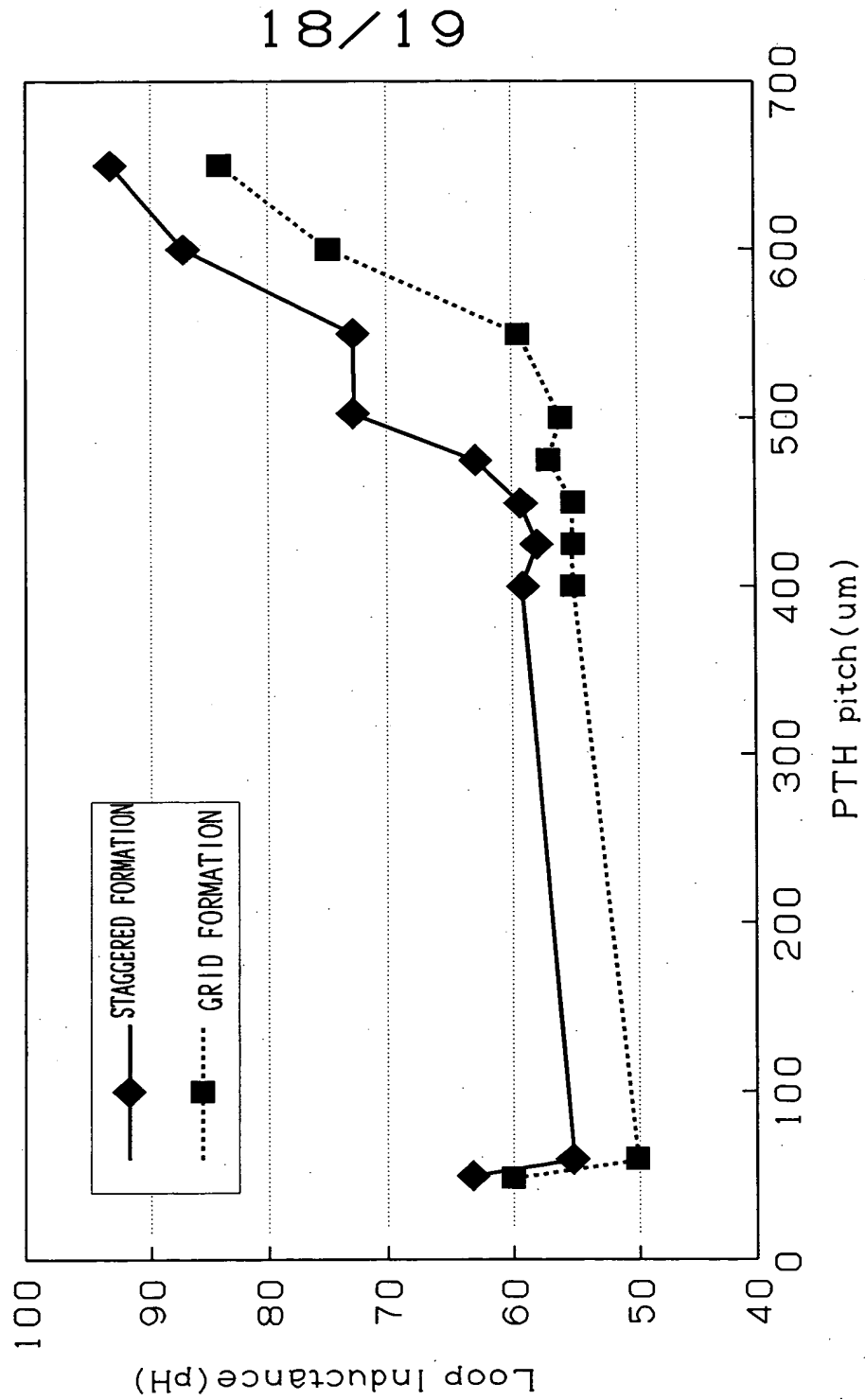
Core thickness = 600 μ m, PTH wall to wall space = 200 μ m

Fig. 19
RATIO OF CORE POWER LAYER

